PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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In re the Application of

Nobuaki HASHIMOTO

Group Art Unit: 3729

Application No.: 09/486,556

Examiner: I. Patel

Filed: February 29, 2000

Docket No.: 105029

For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE THEREOF, CIRCUIT BOARD, AND ELECTRONIC INSTRUMENT

AMENDMENT

Director of the U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

In reply to the August 1, 2001 Office Action, please amend the above-identified application as follows:

IN THE CLAIMS:

Please replace claims 1 and 21 as follows:

1. (Amended) A method of manufacturing a semiconductor device in which a semiconductor chip on which electrodes are formed, and a substrate on which an interconnect pattern is formed and which is covered by a protective layer except a region in said interconnect pattern of electrical connection with said electrodes, are connected by ~~an~~ a conductive adhesive, said method comprising:

a first step of providing said adhesive on said substrate from a region of mounting of said semiconductor chip to said protective layer, said adhesive, said protective layer and said interconnect pattern overlapping with one another outside of said region of mounting of said semiconductor chip; and

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a second step of adhering said substrate to said semiconductor chip by means of said adhesive to electrically connect said interconnect pattern with said electrodes.

21. (Amended) A semiconductor device comprising:

a semiconductor chip having electrodes; a substrate on which an interconnect pattern is formed; a protective layer provided on said substrate excluding a region of said interconnect pattern of electrical connection with said electrodes of said semiconductor chip; and ~~an~~ a conductive adhesive;

wherein said adhesive is provided on said substrate from a region of mounting of said semiconductor chip to said protective layer, said adhesive, said protective layer and said interconnect pattern overlapping with one another outside of said region of mounting of said semiconductor; and

wherein said electrodes of said semiconductor chip are electrically connected with said interconnect pattern.

REMARKS

Claims 1-29 are pending. By this Amendment, claims 1 and 21 are amended to change the language of the claims by reciting that the adhesive, the protective layer and the interconnect pattern overlap with one another outside the region of mounting of the semiconductor chip. No other elements of claims 1 and 29 are affected. No new matter is introduced.

The Office Action rejects claims 21-24, 26, 28 and 29 under 35 U.S.C. §102(e) over Miyata et al. (U.S. Patent No. 6,204,564). This rejection is respectfully traversed.

The Office Action asserts that Miyata discloses all the elements recited in claim 21. However, Applicant respectfully submits that Miyata does not disclose or suggest an adhesive, a protective layer and an interconnected pattern overlap with one another outside the region of mounting of the semiconductor chip, as recited claims 1 and 21.

The Office Action asserts that the alpha-ray shielding insulation layer 25 as shown in Fig. 23 and discussed at col. 15, lines 56-67, reads on the protective layer recited in claims 1 and 21. However, as clearly shown in Figs. 6 and 23, the alpha-layer 25, the adhesive layer 5 and the wiring patterns 21 do not overlap outside the semiconductor mounting area. Thus, Miyata does not disclose or suggest all the features recited in claims 1 and 21.

Claims 21-24, 26, 28 and 29 depend from claim 21. Thus, Miyata does not disclose all the features recited in claims 21-24, 26, 28 and 29. Withdrawal of the rejection of claims 21-24, 26, 28 and 29 under 35 U.S.C. §102(e) is respectfully solicited.

The Office Action rejects claim 25, 1-20 and 27 under 35 U.S.C. §103(a) over Miyata. This rejection is respectfully traversed.

Regarding claim 25, the Office Action asserts that the adhesive that includes a shading material recited in claim 25 would have been obvious because of design choice. However, Applicant respectfully submits that the Office Action is engaging in pure speculation. For example, Miyata does not disclose such a shading material. Instead, Miyata discloses an alpha-ray shielding insulation coating 25 in addition to adhesive material 5. Thus, Miyata does not disclose or suggest adding a shading material, but instead teaches to use a separate layer.

The Office Action is engaging in impermissible hindsight reconstruction using the present application as a road map. There is no applied prior art that discloses or suggests adding a shading material in the adhesive.

Regarding claims 1-20, the Office Action asserts that the method is obvious in view of the product disclosed by Miyata. However, as discussed above, Miyata does not disclose or suggest an adhesive, a protective layer and an interconnected pattern overlap with one another outside the region of mounting of the semiconductor chip, as recited in claim 1. Claims 2-20

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depend form claim 1. Thus, Miyata would not have rendered obvious the subject matter recited in claims 1-20.

Regarding claim 27, the Office Action merely relies on the rejection of claims 1-20. However, as discussed above, Miyata does not disclose or suggest the subject matter recited in claims 1-20. Accordingly, Miyata would not have rendered obvious the subject matter recited in claim 27.

In view of the above, Miyata does not disclose or suggest the subject matter recited in claims 25, 1-20 and 27. Withdrawal of the rejection of claims 25, 1-20 and 27 under 35 U.S.C. §103(a) is respectfully solicited.

For at least the reasons set forth above, Applicant respectfully submits that the application is in condition for allowance. Favorable consideration and prompt allowance of the claims are earnestly solicited. Should the Examiner believe anything further is desirable to place this application in even better condition for allowance, the Examiern is invited to contact Applicants representative at the telephone number listed below.

Respectfully submitted,

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JAO:PT/sld
Attachments:
Appendix
Petition for Extension of Time

Date: November 13, 2001

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